Hussin Abdullah

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EDUCATION

Carleton University, Ottawa, ON
Bachelor of Engineering, Electrical Engineering

TECHNICAL SKILLS

RTL & Digital Design: Verilog, SystemVerilog, FSM Design (Moore/Mealy), Asynchronous FIFO, Clock Gating, Low-Power Design, Synchronous/Asynchronous Reset, Synthesizable RTL

Verification: SystemVerilog Assertions (SVA), Directed Testbenches, Self-Checking Testbenches, Functional Coverage, Lint Closure, CDC Closure, Pre-Silicon Validation, Waveform Debug

Analog & Custom IC: Full-Custom CMOS Layout, Schematic Capture, DRC/LVS, Parasitic Extraction, Multi-Finger Devices, Common-Centroid Layout, PVT Corner Analysis, 45nm SOI

Protocols & Architecture: PCIe Transaction Layer (TLP), Credit Flow Control, Link Power States (L0/L0s/L1), RISC-V (RV32I, PicoRV32), Memory-Mapped I/O, Boot Sequencing, I2C, SPI, UART

Tools: Cadence Virtuoso, Spectre, Questa/ModelSim, Verilator, Quartus Prime, Vivado, Wentworth Probe Station, HP 4155A Analyzer, Tektronix Oscilloscope, Git

Programming: Verilog, SystemVerilog, Python, MATLAB, C, C++, Tcl, Shell Scripting

WORK EXPERIENCE

Data Entry Clerk, *Durham Employment and Newcomer Centre, Toronto, ONJun. 2026 -- Present*

- Evaluated a new in-house appointment management system and authored a structured 32-issue defect and improvement report, presenting findings to the team to drive the remediation backlog.
- Built and maintained Excel tracking databases for client follow-ups and training-funding sources, logging multi-attempt outreach with dated outcomes across all assigned accounts.

PROJECT EXPERIENCE

PCIe Transaction Layer Packet Generator & Checker*Verilog, SystemVerilog, Verilator, Questa*

- Architected and coded 5 synthesizable Verilog modules implementing the PCIe Transaction Layer (encoder, decoder, credit-flow FSM, async FIFO, power FSM) supporting Memory Read, Memory Write, and Completion TLPs across a 250 MHz core and 125 MHz PHY domain.
- Designed a 6-state Moore credit-flow FSM enforcing the PCIe credit protocol, a power FSM with L0/L0s/L1 clock gating, and a dual-clock async FIFO using Gray-code pointers and 2-FF synchronizers sized from a worst-case 2:1 burst analysis to guarantee zero overflow.
- Achieved full lint sign-off in Verilator 5.040 -Wall by root-causing and fixing all 10 warnings at the RTL source with zero blanket waivers; two fixes added functional malformed-packet detection.
- Authored a formal CDC closure report documenting all 5 clock-domain crossings and verified 12 directed TLP transactions through 3 SVA assertions in Questa with 0 violations, mirroring a production ASIC sign-off package.

RISC-V SoC Pre-Silicon Validation Platform*SystemVerilog, Questa/ModelSim, PicoRV32*

- Integrated a PicoRV32 RV32I core with a 9-module SoC in SystemVerilog: a 6-state power-management FSM, 1 KB boot ROM, 4 KB RAM, 256 B memory-mapped PMU registers, and an address-decoding interconnect at 100 MHz.
- Designed a self-checking testbench with real-time boot-stage and PMU-state monitors, validating a deterministic 5-stage boot flow via non-intrusive program-counter tracking.
- Wrote 11 SystemVerilog Assertions covering PMU reachability, forward-only boot progression, 4-byte address alignment, and memory response timing; achieved 100% boot-stage coverage with 0 assertion violations.
- Diagnosed a full-simulation-timeout hang by tracing the CPU program counter in Questa waveforms to cut boot from a 1,000,000-cycle timeout to a clean 2,500 cycles (~25 us).

Custom CMOS IC -- 31-Bit Pseudo-Random Sequence Generator (Fabricated)*Cadence Virtuoso, CuSOI Process*

- Designed and fabricated a full-custom CMOS chip implementing a 5-flip-flop / XNOR-feedback PRSG with an on-chip RC clock oscillator and 10 mA open-drain output driver, built up from transistor-level inverter, NAND, NOR, XNOR, and D-flip-flop cells.
- Engineered transistor sizing and achieved 100% DRC and LVS clean sign-off on the full chip within a 576 x 576 um area constraint.
- Fabricated the die in the Carleton Microfabrication Facility and performed post-silicon bring-up on a Wentworth probe station with an HP 4155A analyzer and Tektronix TDS2024C oscilloscope.
- Measured a working on-chip clock against a simulation target and conducted root-cause analysis of the silicon-vs-simulation gap across power delivery, component tolerance, and signal integrity.

Two-Stage CMOS Operational Amplifier -- 45 nm SOI*Cadence Virtuoso, Spectre*

- Designed and simulated a two-stage CMOS op-amp (differential pair, active-load current mirrors, output buffer) in 45 nm SOI: 20.38 dB gain, 2.043 MHz unity-gain bandwidth, 110.8 deg phase margin, 864.8 uW.
- Executed a full 27-point PVT corner sweep (FF/NN/SS x 1.08/1.2/1.32 V x -40/25/85 C), characterizing gain, bandwidth, phase margin, offset, and slew at every corner.
- Verified robust stability across all corners, with a phase margin above 106 deg and gain variation under 11% against process and environmental shifts.
- Planned a 54-device common-centroid floorplan with dummy transistors and symmetric routing, computing per-row finger counts to equalize finger width across differential and mirror pairs.