TECHNICAL DESIGN REPORT

PCIe Transaction Layer Packet Generator & Checker

RTL Design | CDC Closure | Lint Sign-off | Functional Verification

Hussin Abdullah

Personal Project | February 2026

0 Lint Warnings	5 CDC Crossings	0 Assertion Violations	3 TLP Types
Verilator 5.040 -Wall	All documented & closed	12 TLP transactions	MRd, MWr, Completion

SECTION 1 Abstract & Project Overview

This report documents the complete design, verification, and closure of a synthesizable PCIe Transaction Layer Packet (TLP) Generator and Checker, implemented in Verilog HDL. The project demonstrates industry-standard ASIC design competencies directly aligned with RTL design engineer roles in the semiconductor industry, with particular focus on PCIe IP development as required by positions at companies such as AMD.

The design implements the PCIe Transaction Layer supporting Memory Read, Memory Write, and Completion transaction types across two asynchronous clock domains (250 MHz core and 125 MHz PHY), connected via a Gray-code asynchronous FIFO. A credit-based flow control FSM and a power management controller implementing L0, L0s, and L1 link power states are included.

All deliverables — RTL source, lint closure report, CDC closure report, testbench, and simulation results — mirror the artifacts produced by RTL engineers in production ASIC development. This report is structured as an internal design review document suitable for presentation to a design team.

Project Repository

All source code, documentation, and closure reports: github.com/Ahsent/pcie_tlp_project

SECTION 2 Technical Background — PCIe Protocol

2.1 PCIe Architecture Overview

PCI Express (PCIe) is the dominant high-speed serial interconnect standard used in modern servers, GPUs, SSDs, and network interface cards. The protocol is organized into three layers: Physical (electrical signaling), Data Link (reliability), and Transaction (packet construction). This project implements a subset of the Transaction Layer.

2.2 Transaction Layer Packets

All communication at the Transaction Layer occurs through TLPs. Each TLP consists of a 3 or 4 DWORD header optionally followed by a data payload. This project implements 3DW (96-bit) headers for 32-bit addressing — the most common format for system memory transactions.

TLP Type	Description
Memory Read (MRd)	Non-posted request to read from memory. Requester sends MRd, expects Completion in response. FMT=2'b00.
Memory Write (MWr)	Posted transaction (no response required) writing data to memory. FMT=2'b10.

Completion (Cpl)	Response to a Non-Posted request. Carries requested data or status code. FMT=2'b01, Type=5'b01010.

2.3 Credit-Based Flow Control

PCIe uses credits to prevent receiver buffer overflow. Each receiver advertises a credit count at link initialization. The transmitter may only send if it holds sufficient credit of the appropriate class (Posted, Non-Posted, or Completion). Credits are returned via update DLLPs when the receiver frees buffer space.

2.4 Link Power Management

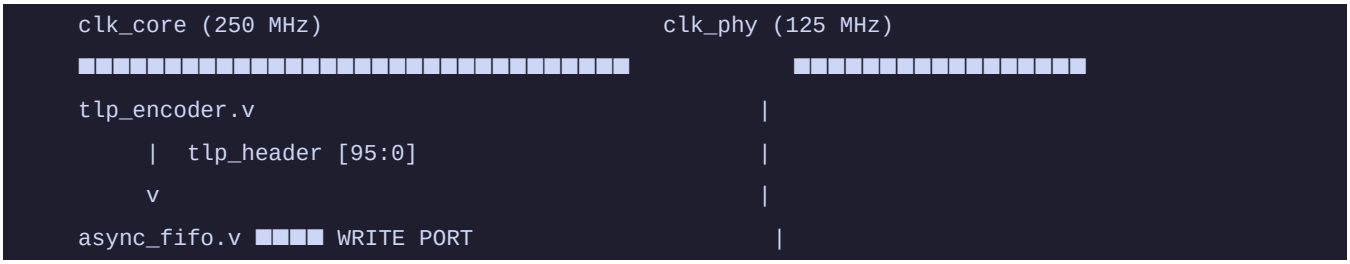
PCIe defines link power states to reduce dynamic power during inactivity. L0 is fully active. L0s gates the datapath clock after 16 idle cycles. L1 enables full clock gating after 64 idle cycles. Dynamic power savings are proportional to 0.5*C*V^2*f per idle flip-flop. The power_fsm module implements these transitions.

SECTION 3 System Architecture

3.1 Top-Level Block Description

Module	Description & Role
tlp_encoder.v	Parameterized TLP header assembler. Single-cycle registered output. Parameter DATA_WIDTH reserved for 128-bit expansion.
tlp_decoder.v	TLP header field extractor with error detection. Asserts decode_err if any reserved field is non-zero.
credit_fsm.v	6-state credit flow control FSM (INIT, IDLE, CHECK_CREDIT, SEND, UPDATE_CREDIT, STALL). Three-block coding style.
async_fifo.v	Dual-clock async FIFO implementing CDC boundary. Gray-code pointers, 2-FF synchronizers, 16-entry depth, 96-bit width.
power_fsm.v	PCIe L0/L0s/L1 power state controller. Asserts clk_gate_en to gate datapath clock in low-power states.

3.2 Clock Domain Architecture



```
        |             Gray-code ptr ■■2FF■■> READ PORT|
        |             2FF <■■■■ Gray-code ptr         |
    tlp_decoder.v                                    |
    credit_fsm.v                                     |
    power_fsm.v                                      |
```

3.3 TLP Header Bit-Field Map

Bit Range	Field	Description
[95:94]	FMT [1:0]	Format: 00=MRd, 10=MWr, 01=Cpl
[93:89]	Type [4:0]	TLP type: 00000=Memory, 01010=Completion
[88]	T9	Reserved — must be 0; checked by decoder
[87:85]	TC [2:0]	Traffic Class — 000 for default
[84:80]	Attr/Flags	Reserved attributes — set to 0
[73:64]	Length [9:0]	Payload length in DWORDs (1-128)
[79:64]	Requester ID	Bus/Device/Function of requesting agent
[63:56]	Tag [7:0]	Transaction identifier
[55:48]	Byte Enables	First and Last DW byte enables
[47:16]	Address [31:0]	32-bit target memory address
[15:0]	Reserved	Set to 0; checked for non-zero by decoder

SECTION 4 RTL Design Details

4.1 TLP Encoder Design

The encoder implements a single-cycle registered architecture. All TLP header fields are assigned to their corresponding bit slices of the 96-bit output register in a single always block, producing one clock cycle of latency between valid_in and valid_out. This latency is deterministic and allows pipelined datapath integration. The DATA_WIDTH parameter is present for future 128-bit expansion.

4.2 Credit FSM State Machine

State	Behaviour
INIT	Loads initial P/NP/CPL credit counts from input ports on first clock after reset.
IDLE	Waits for send_req assertion. Transitions to CHECK_CREDIT when transmission requested.
CHECK_CREDIT	Verifies credit > 0 for the requested TLP class. Transitions to SEND or STALL.
SEND	Asserts send_grant, decrements credit counter. Goes to UPDATE_CREDIT or IDLE.
UPDATE_CREDIT	Adds cred_update to all three credit counters (PCIe credit return). Returns to IDLE.
STALL	Asserts stall for one cycle (no credits). Returns to IDLE to re-evaluate.

4.3 Async FIFO CDC Implementation

The async_fifo module implements the industry-standard dual-clock FIFO architecture. Key design decisions:

- **Gray Code:** Ensures only one bit transitions per pointer increment, eliminating multi-bit glitch hazard when crossing clock domains.
- **2-FF Synchronizers:** Both wr_ptr_gray and rd_ptr_gray pass through two destination-domain flip-flops, providing two full clock periods for metastability resolution.
- **Local Flag Generation:** Full and empty flags are computed within their respective domains from already-synchronized pointers — no flag crosses a clock boundary.
- **Depth Rationale:** 16 entries absorbs burst traffic at 2:1 clock ratio. At maximum write / minimum read rate, 32 clk_phy cycles elapse before overflow at full burst.

4.4 Power FSM Design

The power_fsm uses threshold-based transitions: 16 idle cycles to enter L0s (partial clock gating), 64 cycles to enter L1 (full clock gating). The clk_gate_en output connects to an ICG cell in physical synthesis. In FPGA synthesis (Vivado/Quartus), equivalent clock enable logic is inferred automatically from the enable signal pattern.

SECTION 5 Lint Closure

All five RTL modules were subjected to static lint analysis using Verilator 5.040 with -Wall, activating all available warning categories. Warnings were root-caused and fixed at the RTL level — not suppressed with blanket waivers — until zero warnings remained across all modules.

5.1 Lint Results Summary

Module	Initial Warnings	Final Warnings
tlp_encoder.v	3	0 — CLEAN
tlp_decoder.v	2	0 — CLEAN
credit_fsm.v	2	0 — CLEAN
async_fifo.v	3	0 — CLEAN
power_fsm.v	0	0 — CLEAN

5.2 Notable Findings and Resolutions

Warning	Root Cause & Fix
WIDTHTRUNC (tlp_encoder:32)	Header field concatenation generated 25 bits for a 16-bit target. Fixed by replacing single concatenation with individual bit-slice assignments, making intent explicit.
UNUSEDSIGNAL (tlp_decoder:[87:80],[15:0])	Reserved header fields were silently discarded. Fixed by incorporating them into decode_err logic — functionally correct enhancement checking for PCIe spec violations.
CASEINCOMPLETE (credit_fsm, 2x)	Two case statements missing default branches: tlp_class selector and main state machine. Fixed with default branches eliminating potential latch inference.
MULTIDRIVEN (async_fifo, ptr signals)	Reset and increment logic for pointers split across separate always blocks. Fixed by merging into single always blocks with negedge rst_n — correct async reset coding style.
UNUSEDPARAM (tlp_encoder:DATA_WIDTH)	Parameter not yet used in RTL body. Targeted lint_off/lint_on waiver applied — parameter retained for planned 128-bit expansion.

SECTION 6 CDC Closure

The design contains one CDC boundary between clk_core (250 MHz) and clk_phy (125 MHz), with five signal crossings all contained within the async_fifo module.

6.1 CDC Crossing Inventory

Signal	Direction	Method & Rationale
tlp_header [95:0]	core → phy	Async FIFO data path. Data stable in SRAM before rd_ptr advances. Pointer handshaking guarantees integrity.
wr_ptr_gray [4:0]	core → phy	2-FF synchronizer in rd_clk domain. Gray code ensures single-bit transitions only.
rd_ptr_gray [4:0]	phy → core	2-FF synchronizer in wr_clk domain. Same rationale as above, reverse direction.
full [1]	Within core	No crossing. Computed combinatorially from synchronized rd_ptr entirely in clk_core domain.
empty [1]	Within phy	No crossing. Computed combinatorially from synchronized wr_ptr entirely in clk_phy domain.

6.2 Synchronization Strategy

Gray-code encoding ensures only one pointer bit changes per increment. Even if the receiving domain captures the wrong clock edge due to metastability, it sees either the previous valid pointer or the new valid pointer — never a phantom intermediate address. The 2-FF synchronizer then provides two full destination-clock periods for metastability to resolve. At 250/125 MHz with standard CMOS, this achieves mean-time-between-failures well in excess of the system design lifetime.

CDC Sign-off

All 5 crossings identified, documented, and verified. Single CDC boundary via industry-standard async FIFO with Gray-code + 2-FF synchronizers. No combinational paths cross domain boundaries. Full report: docs/cdc_closure_report.md

SECTION 7 Functional Verification

Verification was performed using a directed SystemVerilog testbench with SVA assertions, simulated in Questa Intel Starter FPGA Edition. The testbench exercises all supported TLP types across a range of payload lengths and addresses, including boundary conditions.

7.1 SVA Assertions

Assertion	Specification Being Checked
p_fmt_match	Decoded FMT field must exactly match the FMT provided to the encoder. Fires on every dec_valid_out cycle. Any mismatch indicates a header assembly or bit-extraction bug.
p_addr_match	Decoded 32-bit address must exactly match the encoder input address. Validates correct bit-slice assignment in both modules.
p_no_err	decode_err must never assert during valid TLP processing. Verifies no reserved fields are inadvertently set by the encoder.

7.2 Test Cases

Test	TLP Type	Vectors
TEST 1	Memory Read (FMT=2'b00)	Lengths: 1, 16, 128 DW. Addresses: 0xA0/B0/C0000000
TEST 2	Memory Write (FMT=2'b10)	Lengths: 1, 16, 128 DW. Addresses: 0xD0/E0/F0000000
TEST 3	Completion (FMT=2'b01,T=5'b01010)	Lengths: 1, 16, 128 DW. Addresses: 0x10/20/30000000
TEST 4	Boundary Cases (MWr + MRd)	Addr 0x00000000, 0xFFFFFFFC, 0xDEADBEF0

Simulation Result

Assertions: 3 active, 0 violations across 12 transactions. dec_err: deasserted throughout all tests. All TLP types verified: MRd, MWr, Completion. Waveform: docs/waveform_screenshot.png

SECTION 8 Skills Demonstrated & Industry Alignment

The table below maps project deliverables to the specific skill requirements in AMD's ASIC Design Engineer role description and general RTL design expectations across the semiconductor industry.

Skill / Requirement	Project Evidence
RTL coding in Verilog HDL	5 synthesizable modules with parameterized datapath. Three-block FSM coding style.
Multiple clock domain design	250/125 MHz dual-domain with async FIFO CDC. Gray-code + 2-FF synchronizers.
Lint tool experience	Verilator 5.040 -Wall. 10 warnings root-caused and fixed. Zero at sign-off.
CDC methodology	Manual CDC closure report: 5 crossings documented with sync method and rationale.
Developing specifications	Block spec written pre-RTL covering interfaces, clock domains, FSMs, assumptions.
High-speed I/O protocol	PCIe TLP header format, credit flow control, power state management.
Low power design	Clock gating via clk_gate_en. L0/L0s/L1 FSM with threshold-based transitions.
Verification & debug	SVA assertions (3), directed test vectors (12), waveform analysis.
FSM design	Two FSMs: 6-state credit controller and 3-state power manager.
Professional documentation	Lint report, CDC report, block spec, design report — all in repository.

SECTION 9 Conclusion

This project demonstrates end-to-end ownership of a digital RTL design from specification through verification — the same workflow followed by ASIC engineers in production IP development. Three aspects distinguish it from typical student projects:

- **Formal closure documents:** The lint and CDC closure reports are the same artifact types that sign off RTL for tape-out in industrial flows. Producing them as a student demonstrates familiarity with real engineering process.
- **Protocol depth:** Implementing PCIe credit-based flow control and power state management requires understanding the PCIe specification architecturally — directly transferable to working on PCIe IP in an ASIC role.
- **RTL quality discipline:** Every lint warning was root-caused and fixed at the RTL level. The MULTIDRIVEN fix on async_fifo and the UNUSEDSIGNAL fix on tlp_decoder made the RTL functionally better, not just quieter.

The project is maintained as a public GitHub repository with a professional README, full documentation, and clean commit history.

Public Repository

github.com/Ahsent/pcie_tlp_project — Available for review by any hiring engineer.

Hussin Abdullah | hussin_abdullah@hotmail.com | www.hussinaltaee.com | linkedin.com/in/hussinaltaee